FAIRCHILD SEMICONDUCTOR®

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FXLA102
Low Voltage Dual Supply 2-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

Features

- Bi-directional interface between two levels from 1.1V to 3.6V.
- Fully configurable: Inputs and outputs track V_{CC} level.
- Non-preferential power-up; either V_{CC} may be powered-up first.
- Outputs remain in 3-state until active V_{CC} level is reached.
- Outputs switch to 3-state if either V_{CC} is at GND.
- Power off protection
- Bushold on data inputs eliminates the need for pull-up or pull-down resistors
- Control input ($\overline{OE}$) is referenced to V_{CCA} voltage.
- Packaged in 8-terminal leadless MicroPak (1.6mm x 1.6mm)
- Direction control not needed.
- 100 Mbps throughput when translating between 1.8V and 2.5V.
- ESD protection exceeds:
  - 15kV HBM (B port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM (A port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 2kV CDM (per ESD STM 5.3)

General Description

The FXLA102 is a configurable dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the V_{CCA} level, and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

The device remains in 3-state until both VCCs reach active levels, allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-state if either V_{CC} is removed.

The $\overline{OE}$ input, when high, disables both the A and B ports by placing them in a 3-state condition. The $\overline{OE}$ input is supplied by V_{CCA}.

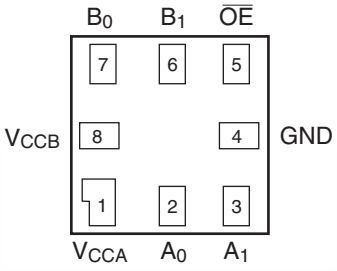
The FXLA102 supports bi-directional translation without the need for a direction control pin. The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
FXLA102L8X	MAC08A	XF	8-Lead MicroPak, 1.6mm Wide	3k Units on Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

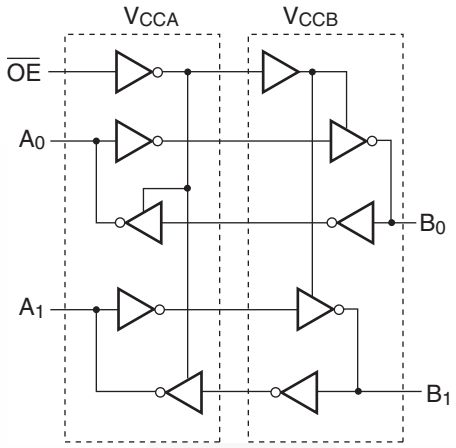


(Top Thru View)

Pin Description

Number	Name	Description
1	V_{CCA}	A Side Power Supply
2, 3	A_0, A_1	A Side Inputs or 3-State Outputs
4	GND	
5	$\overline{OE}$	Output Enable Input
6, 7	B_1, B_0	A Side Inputs or 3-State Outputs
8	V_{CCB}	B Side Power Supply

Functional Diagram



Function Table

Control	
$\overline{OE}$	Outputs
L	Normal Operation
H	3-State

H = HIGH Logic Level

L = LOW Logic Level

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a high-impedance state. The control input ($\overline{OE}$) is designed to track the V_{CCA} supply. A pull-up resistor tying $\overline{OE}$ to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the device driving the $\overline{OE}$ pin.

The recommended power-up sequence is the following:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the $\overline{OE}$ input LOW to enable the device.

The recommended power-down sequence is the following:

1. Drive $\overline{OE}$ input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CCA}, V_{CCB}	Supply Voltage	–0.5V to +4.6V
V_I	DC Input Voltage	
	I/O Port A	–0.5V to +4.6V
	I/O Port B	–0.5V to +4.6V
	Control Input ($\overline{OE}$)	–0.5V to +4.6V
V_O	Output Voltage(2)	
	Outputs 3-STATE	–0.5V to +4.6V
	Outputs Active (A_n)	–0.5V to V_{CCA} + 0.5V
	Outputs Active (B_n)	–0.5V to V_{CCB} + 0.5V
I_{IK}	DC Input Diode Current @ V_I < 0V	–50mA
I_{OK}	DC Output Diode Current @	
	V_O < 0V	–50mA
	V_O > V_{CC}	+50mA
I_{OH} / I_{OL}	DC Output Source/Sink Current	–50mA / +50mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C

Note:

1. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions(2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CCA} or V_{CCB}	Power Supply Operating	1.1V to 3.6V
V_I	Input Voltage	
	I/O Port A	0.0V to 3.6V
	I/O Port B	0.0V to 3.6V
	Control Inputs($\overline{OE}$)	0.0V to V_{CCA}
	Dynamic Output Current I_{OH}/I_{OL} with V_{CC} @	
	3.0V to 3.6V	±12.0mA
	2.3V to 2.7V	±8.0mA
	1.65V to 1.95V	±5.0mA
	1.4V to 1.65V	±3.0mA
	1.1V to 1.4V	±2.0mA
	Static Output Current I_{OH}/I_{OL} with V_{CC} @ 1.1V to 3.6V	±4.0µA
T_A	Free Air Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Maximum Input Edge Rate $V_{CCA/B}$ = 1.1V to 3.6V	10ns/V

Note:

2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

DC Electrical Characteristics (T_A = –40°C to +85°C)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min.	Typ.	Max.	Units
V_{IHA}	High Level Input Voltage	2.7–3.6	1.1–3.6	Data inputs An, Control Input $\overline{OE}$	2.0			V
		2.3–2.7			1.6			
		1.65–2.3			0.65 x V_{CCA}			
		1.4–1.65			0.65 x V_{CCA}			
		1.1 – 1.4			0.9 x V_{CCA}			
V_{IHB}		1.1–3.6	2.7–3.6	Data Inputs Bn	2.0			V
			2.3–2.7		1.6			
			1.65–2.3		0.65 x V_{CCB}			
			1.4–1.65		0.65 x V_{CCB}			
			1.1–1.4		0.9 x V_{CCB}			
V_{ILA}	Low Level Input Voltage	2.7–3.6	1.1–3.6	Data Inputs An, Control Input $\overline{OE}$			0.8	V
		2.3–2.7					0.7	
		1.65–2.3					0.35 x V_{CCA}	
		1.4–1.65					0.35 x V_{CCA}	
		1.1–1.4					0.1 x V_{CCA}	
V_{ILB}		1.1–3.6	2.7–3.6	Data Inputs Bn			0.8	V
			2.3–2.7				0.7	
			1.65–2.3				0.35 x V_{CCB}	
			1.4–1.65				0.35 x V_{CCB}	
			1.1–1.4				0.1 x V_{CCB}	
V_{OHA}[3]	High Level Output Voltage	1.1–3.6	1.1–3.6	I_{OH} = -4µA	V_{CCA} – 0.4			V
V_{OHB}[3]		1.1–3.6	1.1–3.6	I_{OH} = -4µA	V_{CCB} – 0.4			V
V_{OLA}[3]	Low Level Output Voltage	1.1–3.6	1.1–3.6	I_{OL} = 4µA			0.4	V
V_{OLB}[3]		1.1–3.6	1.1–3.6	I_{OL} = 4µA			0.4	V
$I_{I(HOLD)}$	Bushold Input Minimum Drive Current	3.0	3.0	V_{IN} = 0.8V	75.0			µA
		3.0	3.0	V_{IN} = 2.0V	-75.0			
		2.3	2.3	V_{IN} = 0.7V	45.0			
		2.3	2.3	V_{IN} = 1.6V	-45.0			
		1.65	1.65	V_{IN} = 0.57V	25.0			
		1.65	1.65	V_{IN} = 1.07V	-25.0			
		1.4	1.4	V_{IN} = 0.49V	11.0			
		1.4	1.4	V_{IN} = 0.91V	-11.0			
		1.1	1.1	V_{IN} = 0.11V		4		
		1.1	1.1	V_{IN} = 0.99V		-4		
$I_{I(ODH)}$[4]	Bushold Input Overdrive High Current	3.6	3.6	Data Inputs A_n, B_n	450			µA
		2.7	2.7		300			
		1.95	1.95		200			
		1.6	1.6		120			
		1.4	1.4		80			
$I_{I(ODL)}$[5]	Bushold Input Overdrive Low Current	3.6	3.6	Data Inputs A_n, B_n	-450			µA
		2.7	2.7		-300			
		1.95	1.95		-200			
		1.6	1.6		-120			
		1.4	1.4		-80			

DC Electrical Characteristics (T_A = –40°C to +85°C) (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	Conditions	Min.	Typ.	Max.	Units
I_I	Input Leakage Current	1.1–3.6	3.6	Control input $\overline{OE}$, $V_I = V_{CCA}$ or GND			±1.0	µA
I_{OFF}	Power Off Leakage Current	0	3.6	A_n Port, V_O = 0V to 3.6V			±2.0	µA
		3.6	0	B_n Port, V_O = 0V to 3.6V			±2.0	µA
I_{OZ}	3-State Output Leakage	3.6	3.6	Data Outputs A_n, B_n V_O = 0V or 3.6V, $\overline{OE} = V_{IH}$			±5.0	µA
		3.6	0	Data outputs A_n, V_O = 0V or 3.6V, $\overline{OE}$ = GND			±5.0	µA
		0	3.6	Data outputs B_n V_O = 0V or 3.6V, $\overline{OE}$ = GND			±5.0	µA
$I_{CCA/B}$[6][7]	Quiescent Supply Current	1.1–3.6	1.1–3.6	$V_I = V_{CCI}$ or GND, I_O = 0, $\overline{OE}$ = GND			10.0	µA
I_{CCZ}[6][7]	Quiescent Supply Current	1.1–3.6	1.1–3.6	$V_I = VC_{CI}$ or GND, I_O = 0, $\overline{OE} = V_{IH}$			10.0	µA
I_{CCA}	Quiescent Supply Current	0	1.1–3.6	$V_I = V_{CCB}$ or GND, I_O = 0, B-to-A Direction, $\overline{OE}$ = GND			-10.0	µA
		1.1–3.6	0				10.0	µA
I_{CCB}	Quiescent Supply Current	1.1–3.6	0	$V_I = V_{CCA}$ or GND, I_O = 0, A-to-B Direction, $\overline{OE}$ = GND			-10.0	µA
		0	1.1–3.6				10.0	µA

Notes:

3. This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”
4. An external driver must source at least the specified current to switch LOW-to-HIGH.
5. An external driver must source at least the specified current to switch HIGH-to-LOW.
6. V_{CCI} is the V_{CC} associated with the input side.
7. Reflects current per supply, V_{CCA} or V_{CCB}.

Dynamic Output Electrical Characteristics[8]

A Port (An)

Output Load: C_L = 15pF, $R_L \geq 1M\Omega$ ($C_{I/O}$ = 4pF)

		T_A = -40°C to +85°C, V_{CCA} =									
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Units
t_{rise}[9]	Output Rise Time A port		3.0		3.5		4.0		5.0	7.5	ns
t_{fall}[10]	Output Fall Time A port		3.0		3.5		4.0		5.0	7.5	ns
I_{OHD}[9]	Dynamic Output Current High	-11.4		-7.5		-4.7		-3.2		-1.7	mA
I_{OLD}[10]	Dynamic Output Current Low	+11.4		+7.5		+4.7		+3.2		+1.7	mA

B Port (Bn)

Output Load: C_L = 15pF, $R_L \geq 1M\Omega$ ($C_{I/O}$ = 5pF)

		T_A = -40°C to +85°C, V_{CCB} =									
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
Symbol	Parameter	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Units
t_{rise}[9]	Output Rise Time B port		3.0		3.5		4.0		5.0	7.5	ns
t_{fall}[10]	Output Fall Time B port		3.0		3.5		4.0		5.0	7.5	ns
I_{OHD}[9]	Dynamic Output Current High	-12.0		-7.9		-5.0		-3.4		-1.8	mA
I_{OLD}[10]	Dynamic Output Current Low	+12.0		+7.9		+5.0		+3.4		+1.8	mA

Notes:

8. Dynamic Output Characteristics are guaranteed but not tested.
9. See Figure 5.
10. See Figure 6.

AC Characteristics

V_{CCA} = 3.0V to 3.6V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	10.0	ns
	B to A	0.2	3.5	0.2	3.8	0.3	5.0	0.5	6.0	7.0	ns
t_{PZL}, t_{PZH}	$\overline{OE}$ to A, $\overline{OE}$ to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(11)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 2.3V to 2.7V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	10.5	ns
	B to A	0.3	3.9	0.4	4.2	0.5	5.5	0.5	6.5	7.0	ns
t_{PZL}, t_{PZH}	$\overline{OE}$ to A, $\overline{OE}$ to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(11)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.65V to 1.95V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	11.0	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	7.0	ns
t_{PZL}, t_{PZH}	$\overline{OE}$ to A, $\overline{OE}$ to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(11)	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.4V to 1.6V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} =									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
t_{PLH}, t_{PHL}	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	11.5	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	9.0	ns
t_{PZL}, t_{PZH}	$\overline{OE}$ to A, $\overline{OE}$ to B		1.7		1.7		1.7		1.7	1.7	µs
t_{skew}(11)	A Port, B Port		1.0		1.0		1.0		1.0	1.0	ns

Note:

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An, or Bn) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW). Skew is guaranteed but not tested. See Figure 8.

AC Characteristics (Continued)

V_{CCA} = 1.1V to 1.3V

Symbol	Parameter	T_A = -40°C to +85°C, V_{CCB} = 3.0V–3.6V Typ.	2.3V–2.7V Typ.	1.65V–1.95V Typ.	1.4V–1.6V Typ.	1.1V–1.3V Typ.	Units
t_{PLH}, t_{PHL}	A to B	7.1	6.5	7.0	7.1	13.5	ns
	B to A	10.3	10.5	10.8	11.3	13.5	ns
t_{PZL}, t_{PZH}	$\overline{OE}$ to A, $\overline{OE}$ to B	1.7	1.7	1.7	1.7	1.7	µs
t_{skew}(11)	A Port, B Port	1.0	1.0	1.0	1.0	1.0	ns

Note:

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An, or Bn) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW). Skew is guaranteed but not tested. See Figure 8.

Max Data Rate(12)(13)

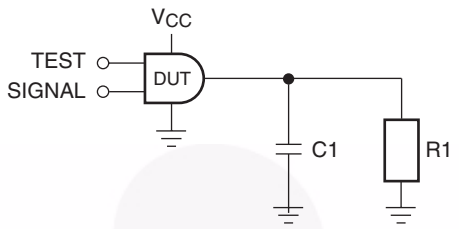
V_{CCA} =	T_A = -40°C to +85°C, V_{CCB} = 3.0V to 3.6V Min.	2.3V to 2.7V Min.	1.65V to 1.95V Min.	1.4V to 1.6V Min.	1.1V to 1.3V Typ.	Units
3.0V to 3.6V	140	120	100	80	40	Mbps
2.3V to 2.7V	120	120	100	80	40	Mbps
1.65V to 1.95V	100	100	80	60	40	Mbps
1.4V to 1.6V	80	80	60	60	40	Mbps
	Typ.	**Typ.**	**Typ.**	**Typ.**	**Typ.**	
1.1V to 1.3V	40	40	40	40	40	Mbps

Note:

12. Max Data Rate is guaranteed but not tested.
13. Max Data Rate is specified in megabits per second. See Figure 7. It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

Capacitance

Symbol	Parameter		Conditions	T_A = +25°C Typical	Units
Cin	Input Capacitance, Control pin ($\overline{OE}$)		V_{CCA} = V_{CCB} = GND	3	pF
Ci/o	Input/Output Capacitance	An	V_{CCA} = V_{CCB} = 3.3V, $\overline{OE}$ = V_{CCA}	4	pF
		Bn		5	
Cpd	Power Dissipation Capacitance		V_{CCA} = V_{CCB} = 3.3V, Vi = 0V or V_{CC}, f = 10MHz	25	pF

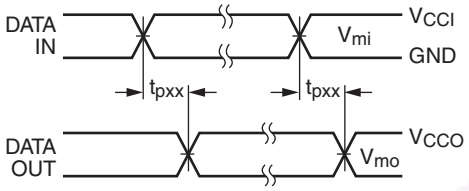


Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	0V
t_{PZL}	0V	HIGH to LOW Switch
t_{PZH}	V_{CCI}	HIGH to LOW Switch

Figure 1. AC Test Circuit

AC Load Table

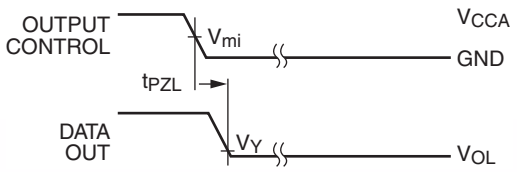
V_{CCO}	CI	RI
1.2V ± 0.1V	15pF	1MΩ
1.5V ± 0.1V	15pF	1MΩ
1.8V ± 0.15V	15pF	1MΩ
2.5V ± 0.2V	15pF	1MΩ
3.3 ± 0.3V	15pF	1MΩ



Input $t_R = t_F$ = 2.0ns, 10% to 90%

Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

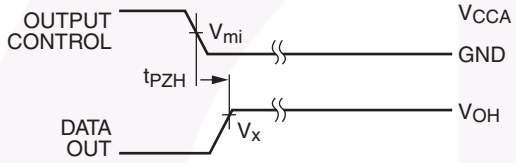
Figure 2. Waveform for Inverting and Non-inverting Functions



Input $t_R = t_F$ = 2.0ns, 10% to 90%

Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

Figure 3. 3-STATE Output Low Enable Time for LOW Voltage Logic



Input $t_R = t_F$ = 2.0ns, 10% to 90%

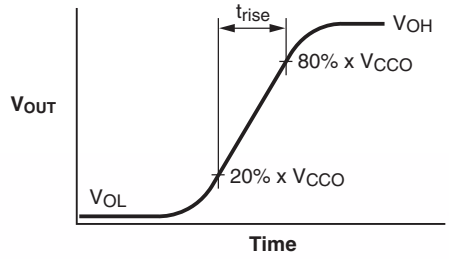
Input $t_R = t_F$ = 2.5ns, 10% to 90%, @ Vi = 3.0V to 3.6V only

Figure 4. 3-STATE Output High Enable Time for LOW Voltage Logic

Symbol	V_{CC}
Vmi(14)	V_{CCI} / 2
Vmo	V_{CCO} / 2
V_X	0.9 x V_{CCO}
V_Y	0.1 x V_{CCO}

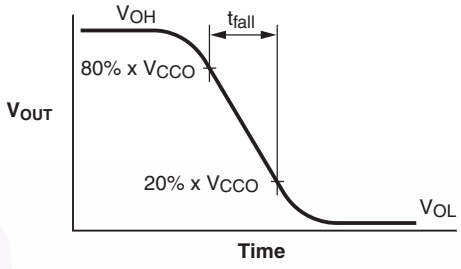
Note:

14. $V_{CCI} = V_{CCA}$ for control pin $\overline{OE}$ or Vmi = (V_{CCA} / 2).



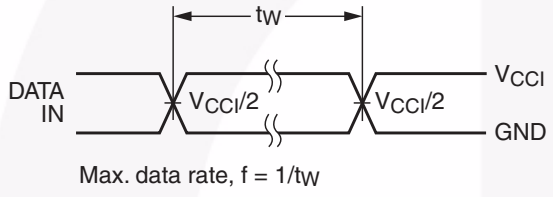
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

Figure 5. Active Output Rise Time and Dynamic Output Current HIGH



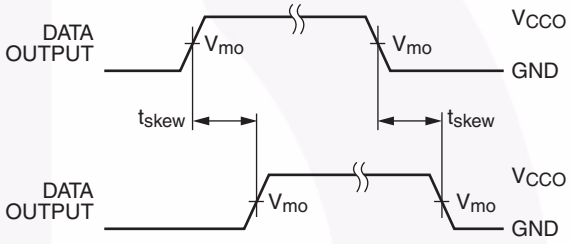
$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

Figure 6. Active Output Fall Time and Dynamic Output Current LOW



Max. data rate, f = $1/t_W$

Figure 7. Maximum Data Rate



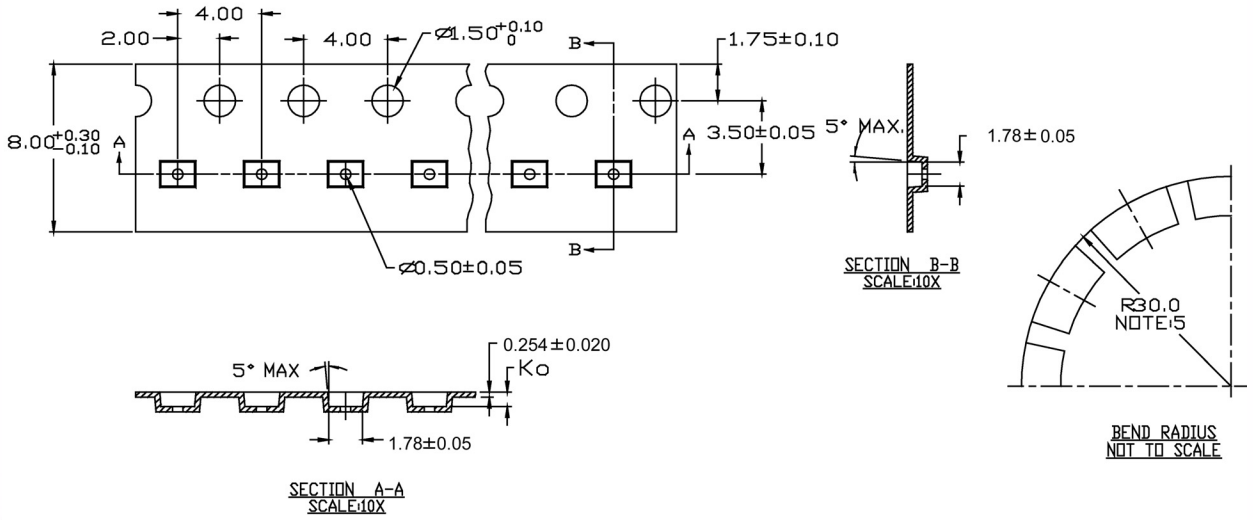
$t_{skew} = (t_{pHLmax} - t_{pHLmin})$ or $(t_{pLHmax} - t_{pLHmin})$

Figure 8. Output Skew Time

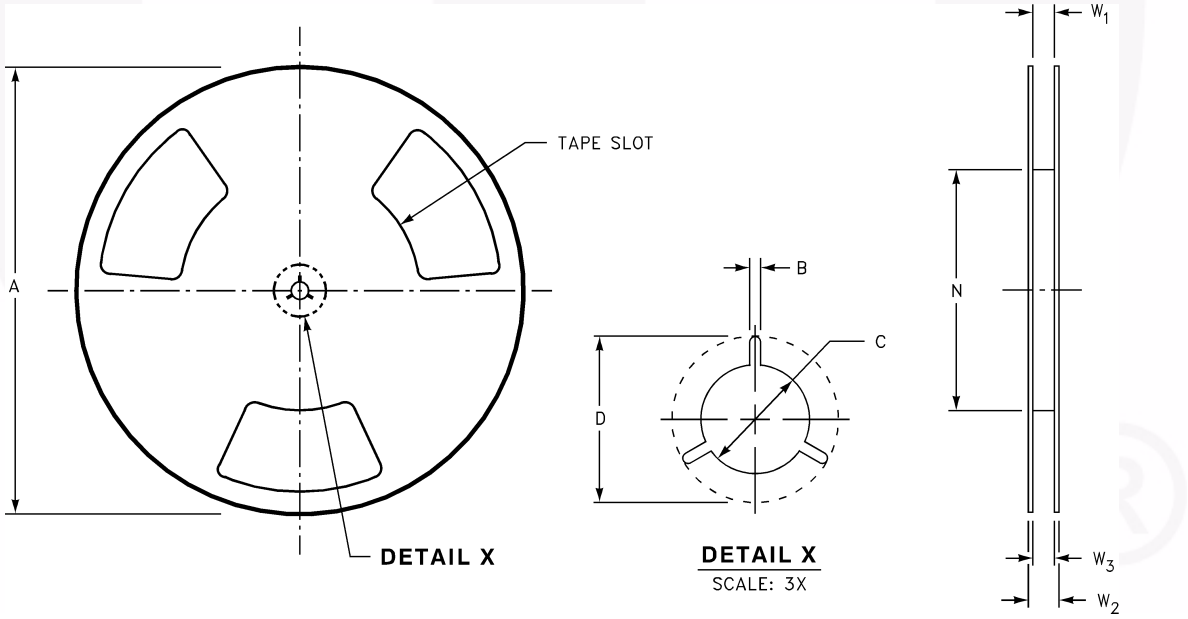
Tape and Reel Dimensions

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions inches (millimeters)

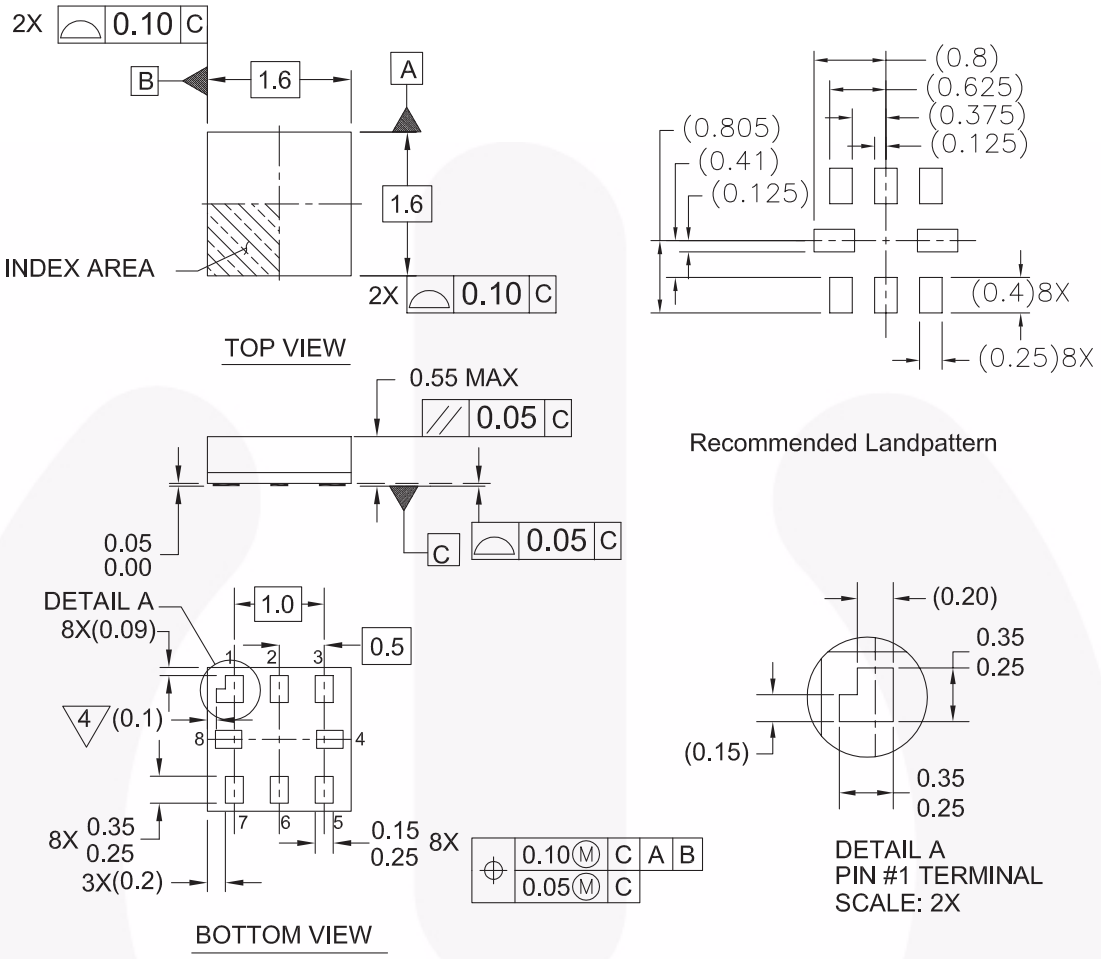


Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 +0.059/–0.000 (8.40 +1.50/–0.00)	0.567 (14.40)	W1 +0.078/–0.039 (W1 +2.00/–1.00)

Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 9. 8-Lead MicroPak, 1.6mm Wide

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